IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	: Helmut Theiler	Art Unit	: 2836
Serial No.	: 10/521,931	Examiner	: Adi Amrany
Filed	: July 19, 2005	Conf. No.	: 2109
Title	: CIRCUIT ARRAY		

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APPEAL BRIEF ON BEHALF OF HELMUT THEILER

Please charge the brief fee of $540 to Deposit Account No. 06-1050. Please apply any other charges or credits to Deposit Account No. 06-1050, referencing Attorney Docket No. 14603-0009US1.

(1) Real Party in Interest

The real party in interest is Austriamicrosystems AG, Schloss Premstatten, A 8141 Unterpremstatten, Austria.

(2) Related Appeals and Interferences

The Appellant is not aware of any appeals or interferences related to the above-identified patent application.

(3) Status of Claims

This is an appeal from the decision of the Examiner in an office action dated November 19, 2008, finally rejecting claims 1-11 and 19-22, all of the claims in the above application.

Claims 12-18 have been withdrawn.

The Appellant filed a Notice of Appeal on January 6, 2009. Claims 1-11 and 19-22 are the subject of this Appeal.

(4) Status of Amendments

All previously filed amendments have been entered.

(5) Summary of Claimed Subject Matter

Claim 1

The Appellant's claim 1 is directed to a circuit array for controlling operation of two loads that operate with a rectified AC voltage. "*To solve this task, a circuit array for controlling two independent loads operable with rectified AC voltage is used in electric devices.*"[1]

Inventive features of the Appellant's claim 1 include a first current path that includes a first load of the two loads, and a second current path that includes a second load of the two loads.[2]

Inventive features of the Appellant's claim 1 also include a semiconductor switch on a circuit path that includes the two loads, the semiconductor switch being electrically connected to a common node of the first current path and the second current path. "*Thus, an electric device, which requires only one MOSFET 14 to control two independent loads, can be executed with the circuit array according to the invention.*"[3]

Inventive features of the Appellant's claim 1 also include a control unit to generate a switch control signal that controls the semiconductor switch. ". . . [A] *circuit array for controlling two independent loads, operable with rectified AC voltage, having a control unit for generating a control signal for a semiconductor switch, by means of which the two loads are each controllable.*"[4]

Inventive features of the Appellant's claim 1 also include a phase detection device to detect whether a phase of the AC voltage is positive or negative, and to output a logical detection

[1] Specification, page 1, lines 16-17.
[2] Figure 3.
[3] Id., page 8, lines 6-7. *See also* Figure 3.
[4] Id., page 3, lines 5-8.

signal that is based on whether the phase is positive or negative. "*The circuit array 1 contains a control device 9 and a phase detection device 6. The phase detection device 6 detects, based on the ripple of the input voltage, whether the diode D1 is admitting a positive half-wave or whether a negative half-wave is being applied. The phase detection device 6 provides, at its output, an output signal 16.*"[5]

Inventive features of the Appellant's claim 1 also include a logic unit to generate the switch control signal based on one or more logical load control signals and the logical detection signal, wherein the control unit is configured to supply the first current path with a first half wave of the rectified AC voltage and to supply the second current path with a second half wave of the rectified AC voltage. "*. . . a positive half-wave is signaled with a logical "1", and that the semiconductor switch 4, in the present exemplary embodiment an N-channel MOSFET, is to be connected when the time control 7 also issues a "1". As a result of the inversion, the other AND element receives a logical "0" in the case of a positive half-wave . . . The principle of the circuit shown in Figure 2 is shown again in Figure 3 in a simple, schematic depiction, wherein an N-channel MOSFET is again used as a semiconductor switch 14.*"[6]

Claim 6

The Appellant's claim 6 is directed to an electronic device. "*For this reason, the circuit array according to the invention is used in an electric device. . . .*"[7]

Inventive features of the Appellant's claim 6 also include a circuit array for controlling a switch to apply voltage to first and second loads based on whether a phase of the AC voltage is

[5] Id., page 5, lines 8-11.
[6] Id., page 6, lines 16-21; page 8, lines 11-13.
[7] Id., page 3, lines 21-22.

positive or negative and logical load control signals generated separately for the first and second loads. ". . . *[t]he control unit contains a phase detection device, by means of which a positive or negative phase of the AC voltage is detectable, and which furnishes an output signal describing the current phase.*"[8] "*In the present case, it is assumed that the presence of a positive half-wave is signaled with a logical "1", and that the semiconductor switch 4, in the present exemplary embodiment an N-channel MOSFET, is to be connected when the time control 7 also issues a "1". As a result of the inversion, the other AND element receives a logical "0" in the case of a positive half-wave. Thus, in the case of a positive half-wave, it is impossible to obtain a "1" at the output of the AND element connected to the sensor unit 8, even when the control signal 18 signals a logical "1". The relationships are reversed in the case of a negative half-wave. In other words, the logic unit 19 consisting of the logic elements described above causes the time control 7 default value to be taken into account during the positive half-wave, while the sensor circuit 8 default value is taken into account during the negative half-wave.*" [9]

Inventive features of the Appellant's claim 6 also include a rectifier that is connected to the input and that provides the voltage to the first and second loads, the voltage being generated from the AC voltage. "*In this connection, a rectifier diode D1 is connected to an AC voltage input 20. The half-waves admitted by the diode D1 are available as a power supply for the circuit array 1, on the one hand, as well as to the loads 2 and 3.*"[10]

Inventive features of the Appellant's claim 6 also include that the rectifier comprises an open bridge circuit.[11] ". . . *[A] rectifier is executed in an open bridge circuit.*"

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[8] Id., page 3, lines 8-11.
[9] Id., page 6, line 17 - page 7, line 7.
[10] Id., page 4, lines 19-22.
[11] Id., page 7, line 10.

Inventive features of the Appellant's claim 6 also include that the voltage comprises different half waves of the AC voltage wherein a first half wave of the rectified AC voltage is applied to the first load and a second half wave of the rectified AC voltage is applied to the second load. *"The voltage tap for the circuit array 11 and therefore for the phase detection device 6 is at the cathode of diode D12; in other words, the phase at the DC voltage output 22 is used for detection. As a result, the detection of a positive half-wave signifies that a current only flows through the heating resistor 2 during this half-wave. Thus, the control signal of the time circuit 7, which can only be taken into account during a positive semiconductor, as described above, only affects the heating resistor 2, because current cannot flow through the lamp 3. The situation is reversed in the case of a negative half-wave, which means that the sensor circuit 8 can only affect the switched state of the lamp 3."*[12]

(6) Grounds of Rejection to be Reviewed on Appeal

1. Claims 6, 9, and 11 stand rejected under 35 U.S.C. 102(b) as being anticipated by Peil (US 4,560,909) ("Peil").

2. Claims 1-11 and 19-22 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Dalnodar (US 5,504,400) ("Dalnodar").

[12] Id., page 7, line 18 – page 8, line 4.

(7) Argument

Anticipation

"It is well settled that anticipation under 35 U.S.C. §102 requires the presence in a single reference of all of the elements of a claimed invention." *Ex parte Chopra*, 229 U.S.P.Q. 230, 231 (BPA&I 1985) and cases cited.

"Anticipation requires the presence in a single prior art disclosure of all elements of a claimed invention arranged as in the claim." *Connell v. Sears, Roebuck & Co.*, 220 U.S.P.Q. 193, 198 (Fed. Cir. 1983).

"This court has repeatedly stated that the defense of lack of novelty (i.e., 'anticipation') can only be established by a single prior art reference which discloses each and every element of the claimed invention." *Structural Rubber Prod. Co. v. Park Rubber Co.*, 223 U.S.P.Q. 1264, 1270 (Fed. Cir. 1984), citing five prior Federal Circuit decisions since 1983 including *Connell*.

In a later analogous case the Court of Appeals for the Federal Circuit again applied this rule in reversing a denial of a motion for judgment n.o.v. after a jury finding that claims were anticipated. *Jamesbury Corp. v. Litton Industrial Prod., Inc.*, 225 U.S.P.Q. 253 (Fed. Cir. 1985).

After quoting from *Connell*, "Anticipation requires the presence in a single prior art disclosure of all elements of a claimed invention arranged as in the claim," 225 U.S.P.Q. at 256, the court observed that the patentee accomplished a constant tight contact in a ball valve by a lip on the seal or ring which interferes with the placement of the ball. The lip protruded into the area where the ball will be placed and was thus deflected after the ball was assembled into the valve. Because of this constant pressure, the patented valve was described as providing a particularly good seal when regulating a low pressure stream. The court quoted with approval

from a 1967 Court of Claims decision adopting the opinion of then Commissioner and later Judge Donald E. Lane:

> [T]he term "engaging the ball" recited in claims 7 and 8 means that the lip contacts the ball with sufficient force to provide a fluid tight seal **** The Saunders flange or lip only sealingly engages the ball 1 on the upstream side when the fluid pressure forces the lip against the ball and never sealingly engages the ball on the downstream side because there is no fluid pressure there to force the lip against the ball. The Saunders sealing ring provides a compression type of seal which depends upon the ball pressing into the material of the ring. *** The seal of Saunders depends primarily on the contact between the ball and the body of the sealing ring, and the flange or lip sealingly contacts the ball on the upstream side when the fluid pressure increases. 225 U.S.P.Q. at 258.

Relying on *Jamesbury*, the ITC said, "Anticipation requires looking at a reference, and comparing the disclosure of the reference with the claims of the patent in suit. A claimed device is anticipated if a single prior art reference discloses all the elements of the claimed invention as arranged in the claim." *In re Certain Floppy Disk Drives and Components Thereof*, 227 U.S.P.Q. 982, 985 (U.S. ITC 1985).

Obviousness

"It is well established that the burden is on the PTO to establish a prima facie showing of obviousness, *In re Fritsch*, 972 F.2d. 1260, 23 U.S.P.Q.2d 1780 (C.C.P.A., 1972)."

In *KSR Intl. Co. v. Teleflex Inc.*, 127 S.Ct. 1727 (2007), the Supreme Court reversed a decision by the Court of Appeal's for the Federal Circuit decision that reversed a summary judgment of obviousness on the ground that the district court had not adequately identified a motivation to combine two prior art references. The invention was a combination of a prior art

repositionable gas pedal, with prior art electronic (rather than mechanical cable) gas pedal position sensing. The Court first rejected the "rigid" teaching suggestion motivation (TSM) requirement applied by the Federal Circuit, since the Court's obviousness decisions had all advocated a "flexible" and "functional" approach that cautioned against "granting a patent based on the combination of elements found in the prior art."

In *KSR* the Supreme Court even while stating that: "the Court of Appeals drew the wrong conclusion from the risk of courts and patent examiners falling prey to hindsight bias," warned that: "a factfinder should be aware, of course, of the distortion caused by hindsight bias and must be cautious of arguments reliant upon *ex post* reasoning."

> The Court of Appeals, finally, drew the wrong conclusion from the risk of courts and patent examiners falling prey to hindsight bias. A factfinder should be aware, of course, of the distortion caused by hindsight bias and must be cautious of arguments reliant upon *ex post* reasoning. See *Graham*, 383 U. S., at 36 (warning against a "temptation to read into the prior art the teachings of the invention in issue" and instructing courts to "'guard against slipping into the use of hindsight'" (quoting *Monroe Auto Equipment Co. v. Heckethorn Mfg. & Supply Co.*, 332 F. 2d 406, 412 (CA6 1964))). Rigid preventative rules that deny factfinders recourse to common sense, however, are neither necessary under our case law nor consistent with it.

With respect to the genesis of the TSM requirement, the Court noted that although "As is clear from cases such as Adams[13], a patent composed of several elements is not proved obvious merely by demonstrating that each of its elements was, independently, known in the prior art. Although common sense directs one to look with care at a patent application that claims as innovation the combination of two known devices according to their established functions, it can be important to identify a reason that would have prompted a person of ordinary skill in the

[13] United States v. Adams, 383 U. S. 39, 40 (1966).

relevant field to combine the elements in the way the claimed new invention does. This is so because inventions in most, if not all, instances rely upon building blocks long since uncovered, and claimed discoveries almost of necessity will be combinations of what, in some sense, is already known."

"The mere fact that the prior art could be so modified would not have made the modification obvious unless the prior art suggested the desirability of the modification." *In re Gordon*, 221 U.S.P.Q. 1125, 1127 (Fed. Cir. 1984).

> Although the Commissioner suggests that [the structure in the primary prior art reference] could readily be modified to form the [claimed] structure, "[t]he mere fact that the prior art could be so modified would not have made the modification obvious unless the prior art suggested the desirability of the modification." *In re Laskowski*, 10 U.S.P.Q. 2d 1397, 1398 (Fed. Cir. 1989).

"The claimed invention must be considered as a whole, and the question is whether there is something in the prior art as a whole to suggest the desirability, and thus the obviousness, of making the combination." *Lindemann Maschinenfabrik GMBH v. American Hoist & Derrick*, 221 U.S.P.Q. 481, 488 (Fed. Cir. 1984).

> Obviousness cannot be established by combining the teachings of the prior art to produce the claimed invention, absent some teaching or suggestion supporting the combination. Under Section 103, teachings of references can be combined only if there is some suggestion or incentive to do so. *ACS Hospital Systems, Inc. v. Montefiore Hospital*, 221 U.S.P.Q. 929, 933 (Fed. Cir. 1984) (emphasis in original, footnotes omitted).

"The critical inquiry is whether 'there is something in the prior art as a whole to suggest the desirability, and thus the obviousness, of making the combination.'" *Fromson v. Advance Offset Plate, Inc.*, 225 U.S.P.Q. 26, 31 (Fed. Cir. 1985).

I. Claim 6, 9, and 11 are not anticipated by Peil.

For the purposes of this appeal only, claims 6, 9, and 11 stand or fall together. The Appellant's claim 6 is representative of this group of claims.

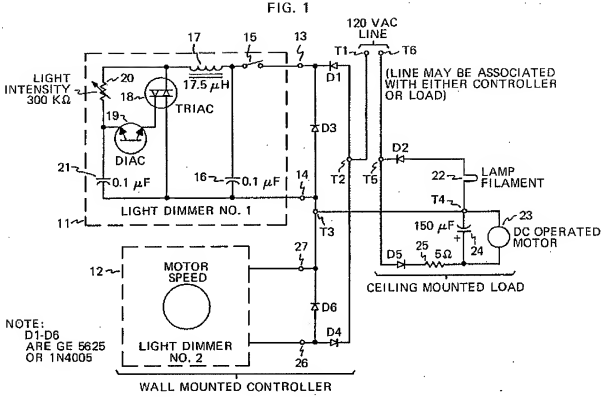
Claim 6 recites an electronic device that includes "a circuit array for controlling a switch to apply voltage to first and second loads based on whether a phase of the AC voltage is positive or negative and logical load control signals generated separately for the first and second loads."[14]

Peil does not describe logical load control signals generated separately for the first and second loads for multiple reasons.

First, Peil fails to describe or suggest "logical" load control signals. Instead, Peil discloses an arrangement "for controlling the power applied to two remote loads energized from a common AC line."[15] As shown in the Figure 1 of Peil below, Peil also includes "a manually adjustable phase shift network including the manually variable resistor 20, and a capacitor 21."[16]

[14] Appellant's claim 6 (emphasis added).
[15] Peil, Abstract.
[16] Id., col. 4 lines 4-6.

FIG. 1



The Examiner argues that: **"Peil discloses an electronic device (fig 1; col. 3-5) comprising . . . logical load control signals (20) generated separately for the first and second loads . . . ."**[17] The Appellant disagrees. In Figure 1 of Peil (shown above), the Examiner refers to element 20, which is described in Peil to be a "manually variable resistor."[18] In describing the function of the phase shift network Peil states:

> The output of the phase shift network available at the interconnected terminals of 20 and 21 is coupled via the diac 19 to the triac 18, as earlier noted. The diac is bidirectionally conductive, breaking down in either direction, when a predetermined breakdown voltage is exceeded. Assuming that the voltage produced in the phase shift network momentarily exceeds that required to break down the diac, a trigger voltage will be

[17] Office Action dated November 19, 2008, page 3.
[18] Peil, col. 4, lines 5-6.

> coupled to the triac causing it to conduct as some point in the ac wave. Conduction by the diac 19 partially discharges the capacitor 21 into the gate of the triac 18.[19]

The Appellant's claim 6 requires that the load control signals are logical signals. In contrast, Peil discloses a load control signal that is delivered by a manually variable resistor 20. Variable resistors, or "potentiometers" are used to adjust the level of analog signals. Accordingly, the analog signal produced by Peil's manually variable resistor 20 is not a "logical" load control signal, as required by the Appellant's claim 6.

Claim 6 also recites that the logical load control signals are "generated separately for the first and second loads." Peil also fails to disclose this feature of claim 6.

In contrast, Peil is understood to describe an arrangement which utilizes the "symmetrical conduction property between successive half waves."[20] The control signals in Peil are not generated separately as required by the Appellant's claim 6. Instead, Peil discloses that two controllers controlled by a single signal control the power provided to two different loads. In this regard, Peil states:

> The . [*sic*] operation of a double power controller with a double load in which one controller operates on positive half waves of the ac waveform to control power to one load and a second controller operates on negative half waves of the ac waveform to control power to a second load will now be described.[21]

Accordingly, Peil discloses that the two load controllers are driven by a single AC waveform, and not by logical load control signals that are generated separately for each load. Therefore, the Appellant requests that the 35 U.S.C. 102(b) rejection of claim 6 be withdrawn.

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[19] Peil, col. 5 lines 27-38.
[20] Id., col 6, lines 11-12.
[21] Id., col. 6, lines 12-18.

II. Claims 1-11 and 19-21 are patentable over Dalnodar.

Claim 1

For the purposes of this appeal only, claims 1-5, 8-11, and 20 stand or fall together. Claim 1 is representative of this group of claims.

Claim 1 was rejected as being unpatentable over over Dalnodar (US 5,504,400). Claim 1 recites, among other limitations, "a logic unit to generate the switch control signal based on one or more logical load control signals and the logical detection signal." Dalnodar fails to disclose or suggest such a logic unit.

First, claim 1 requires that the switch control signal be generated by the logic unit based on at least two signals, namely "one or more logical load control signals and the logical detection signal." In the current rejection, the Examiner compares Dalnodar's diac (DC1) to the claimed logic unit.[22] However, a diac (such as Dalnodar's DC1) is a two terminal device that allows current to flow when a voltage across the two terminals is greater than a breakdown voltage of the device. As shown in Fig. 4 of Dalnodar (reproduced below), the diac DC1 includes a single input (the voltage, v_c, at the node above C1) and a single output (the voltage supplied to the gate 17 of triac T1).

[22] Office Action dated November 19, 2008, page 5.

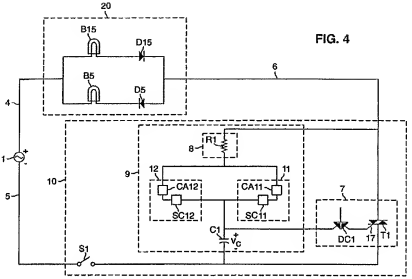

FIG. 4

Regarding the functionality of the diac (DC1) and the triac (T1), Dalnodar states:

> The triac T1 may be triggered into conduction during each half cycle if the voltage v_c across the capacitor C1 is sufficiently high such that the diac DC1 breaks down and partially discharges the capacitor into the gate 17 of triac T1.[23]

As such, in contrast to the claimed invention which requires at least two inputs, in Dalnodar, only a single input is provided to the diac DC1, namely, the voltage across capacitor C1. Thus, the output signal (17) generated by Dalnodar's diac is not "based on one or more logical load control signals and the logical detection signal" as recited in the Appellant's claim 1.

Further, claim 1 requires that the logical unit generate the switch control signal based on "one or more logical load control signals and the logical detection signal." In contrast to the claimed logical load control signals and logical detection signal, Dalnodar describes an analog signal. In this regard, the Examiner concedes that **"Dalnodar discloses that analog signals are passed from the phase detectors (11, 12) to the diac (DC1)."**[24] The analog signal which provides the input to

[23] Dalnodar, col. 5, lines 52-55.
[24] Office Action of November 11, 2008, page 5.

Dalnodar's diac DC1 is the voltage across capacitor C1 (an analog voltage) which is generated based on the values of potentiometers VR11 and VR12. In this regard, Dalnodar states:

> Current will therefore flow through the potentiometer VR11 and the resistance of the potentiometer VR11 will control the charge rate of the capacitor C1. If the potentiometer VR11 is set to its maximum value, then the current charging the capacitor will be at its minimum value. As a result, the voltage v_c will be insufficient to break down the diac DC1, and the triac T1 will not be switched into conduction. As the resistance setting of the potentiometer VR11 is reduced, a larger current will flow... causing capacitor C1 to charge faster such that the voltage v_c will become sufficient to break down the diac DC1 at some point late in the half cycle.[25]

Dalnodar further states:

> This implies that voltage v_c will be non zero at the end of the half cycle. Furthermore, if the voltage v_c was not sufficient to break down the diac DC1 than the capacitor C1 will not have partially discharged, and the voltage at the end of the half cycle may be any value less than the break down voltage of the diac DC1.[26]

As such, in contrast to the Appellant's claimed logical signals, in Dalnodar the load control signal delivered by the capacitor C1 to diac DC1 is analog.

The Examiner attempts to overcome this acknowledged deficiency of Dalnodar by asserting:

> **Dalnodar discloses that analog signals are passed from the phase detectors (11,12) to the diac (OC1). Dalnodar also discloses that the diac converts this signal to a digital signal in order to control the switching of the triac (T1). At the time of the invention by applicant, it would have been obvious to add additional diacs to the Dalnodar circuit in order to convert the signal to digital one step earlier, since it has been held that the mere duplication of the essential working parts of a device involves only routine skill in the art. Sf. Regis Paper Co. v. Bemis Co., 193 USPQ 8 (CCPA 1977).**[27]

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[25] Dalnodar, col. 5, line 65 - col. 6, line 9.
[26] Id., col. 6, line 65 - col. 6, line 3.
[27] Office Action of November 11, 2008, pages 5-6.

To the best of the Appellant's understanding, the Examiner appears to suggest that it would have been obvious to add two additional diacs to Dalnodar's circuit between the variable resistors VR11 and VR12 and the capacitor C1. However, inserting diacs in such a location would no longer allow Dalnodar's circuit to function appropriately because the capacitor C1 would no longer be charged in the same manner. Rather, if such diacs were added, the capacitor would only be charged when the voltage across the resistor VR11 or VR12 exceeded the breakdown voltage of the diac (see discussion above re charging/discharging of capacitor C1).

Furthermore, referring to Figure 4 of Dalnodar (reproduced below), "the triggering circuit 9 includes a capacitor C1, a positive half-cycle charge-rate control circuit 11, a negative half-cycle charge-rate control circuit 12."[28] One terminal of capacitor C1 is connected to a node shared between the output of positive half-cycle charge-rate control circuit 11 and the negative half-cycle charge-rate control circuit 12, and the other terminal of capacitor C1 is connected to conductor 5 between switch S1 and triac T1.

[28] Dalnodar, col. 5, lines 6-9.

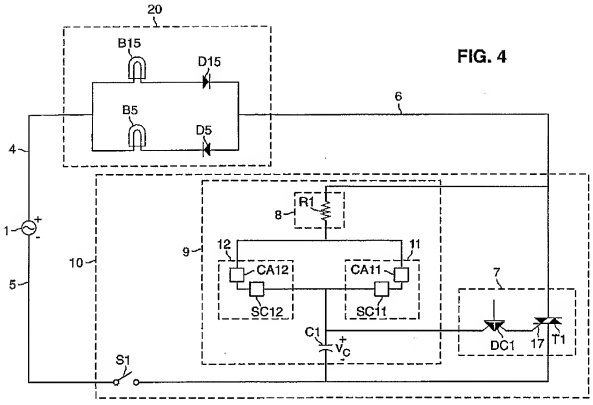


FIG. 4

If two additional diacs were added to Dalnodar's circuit at the outputs of both the positive half-cycle charge-rate control circuit 11 and the negative half-cycle charge-rate control circuit 12, the current flow through triac T1 would be disrupted, as capacitor C1 would block DC signals once charged up to the applied DC voltage. In normal operation, the circuit shown in Figure 4 of Dalnodar passes alternating current through capacitor C1, as AC signals flow through capacitors unimpeded because the capacitor will charge and discharge as the alternating current fluctuates, making it appear that the alternating current is flowing.

Again, in attempting to remedy the deficiency of Dalnodar, the Examiner argues that:

> **Dalnodar discloses that analog signals are passed from the phase detectors (11,12) to the diac (OC1). Dalnodar also discloses that the diac converts this signal to a digital signal in order to control the switching of the triac (T1). At the time of the invention by applicant, it would have been obvious to add additional diacs to the Dalnodar circuit in order to convert the signal to**

digital one step earlier, since it has been held that the mere duplication of the essential working parts of a device involves only routine skill in the art. Sf. Regis Paper Co. v. Bemis Co., 193 USPQ 8 (CCPA 1977).[29]

Appellant contends that this motivation is nothing more than an exercise in *ex post* reasoning. The motivation articulated by the Examiner does not explain how Dalnodar could usefully be modified by converting Dalnodar's analog signal to a digital signal. Rather, the modification appears to be occasioned from reference to Appellant's claims and or specification. The Supreme Court in *KSR Intl. Co. v. Teleflex Inc.*, 127 S.Ct. 1727 (2007), even while stating that: "the Court of Appeals drew the wrong conclusion from the risk of courts and patent examiners falling prey to hindsight bias," warns that: "a factfinder should be aware, of course, of the distortion caused by hindsight bias and must be cautious of arguments reliant upon *ex post* reasoning."

> The Court of Appeals, finally, drew the wrong conclusion from the risk of courts and patent examiners falling prey to hindsight bias. A factfinder should be aware, of course, of the distortion caused by hindsight bias and must be cautious of arguments reliant upon *ex post* reasoning. See *Graham*, 383 U. S., at 36 (warning against a "temptation to read into the prior art the teachings of the invention in issue" and instructing courts to "'guard against slipping into the use of hindsight'" (quoting *Monroe Auto Equipment Co. v. Heckethorn Mfg. & Supply Co.*, 332 F. 2d 406, 412 (CA6 1964))). Rigid preventative rules that deny factfinders recourse to common sense, however, are neither necessary under our case law nor consistent with it.[30]

The Examiner lays no basis for his conclusion that **" it would have been obvious to add additional diacs to the Dalnodar circuit in order to convert the signal to digital one step earlier."** For the reasons discussed above, modifying Dalnodar in the manner suggested by the Examiner would

[29] Office Action of November 11, 2008, pages 5-6.
[30] KSR Intl. Co. v. Teleflex Inc., 127 S.Ct. 1727, 1742-43.

disrupt the described operation of Dalnodar. Therefore, the Examiner's motivation to modify Dalnodar is clearly *ex post* reasoning, that is, application of improper hindsight reconstruction, because the Examiner could have only gleaned the advantages of the novel combination of the elements set forth in the Appellant's claims by using the Appellant's claims and/or specification as a roadmap.

Accordingly, for the foregoing reasons, it would not have been obvious to place additional diacs in Dalnodar's circuit. Furthermore, placing additional diacs in Dalnodar's circuit at the locations suggested by the Examiner would alter the manner in which the device functions. Therefore, the Appellant respectfully requests the rejection of claim 1 be withdrawn.

Claim 6

Claim 6 was rejected as being unpatentable over over Dalnodar (US 5,504,400). Claim 6 recites, among other limitations, "a circuit array for controlling a switch to apply voltage to first and second loads based on whether a phase of the AC voltage is positive or negative and logical load control signals generated separately for the first and second loads." Dalnodar fails to disclose or suggest at least these features of claim 6.

As stated previously, Dalnodar neither describes nor renders obvious logical load control signals. In contrast to the claimed logical load control signals, Dalnodar describes an analog signal. In this regard, the Examiner concedes that **"Dalnodar discloses that analog signals are passed from the phase detectors (11, 12) to the diac (DC1)."** The Examiner attempts to overcome this acknowledged deficiency of Dalnodar by asserting:

> **As discussed above, it would have been obvious to duplicate the Dalnodar diac. Id. Dalnodar discloses that the rectifier is "downstream" of the loads. At the time of the invention by applicant, it would have been obvious to one**

skilled in the art to switch the bulbs (B5, B15) and diodes (05, 015), since it has been held that rearranging parts of an invention involves only routine skill in the art. In re Japikse, 86 USPQ 70 (CCPA 1950). Switching the bulbs and diodes will not affect the performance of the Dalnodar device. The diodes will still direct one of two half waves to each load.[31]

Again, the Examiner appears to suggest that it would have been obvious to add two additional diacs to Dalnodar's circuit between the variable resistors VR11 and VR12 and the capacitor C1. However, inserting diacs in such a location would not have been obvious for the same reasons described above with regard to claim 1. Namely, as described in detail above, the architecture proposed by the Examiner would no longer allow Dalnodar's circuit to function appropriately because the capacitor C1 would no longer be charged in the same manner.

Accordingly, Dalnodar neither describes nor renders obvious the logical load control signals recited in claim 6.

Claim 6 also recites that the logical load control signals are generated separately for the first and second loads. Dalnodar fails to describe or make obvious this feature of claim 6.

In contrast, Dalnodar describes a single load control signal that may have either a positive or negative phase. Again, using Figure 4 of Dalnodar as an example, the load control signal is generated at capacitor C1.

[31] Id., page 8.

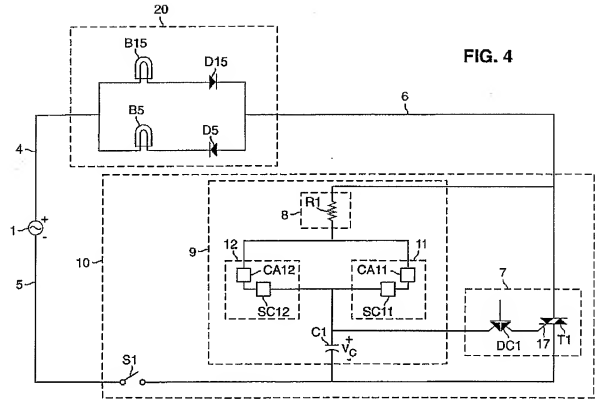


FIG. 4

The analog output of C1 flows through diac DC1 and controls the gate of triac T1. At the end of a positive cycle, the voltage of the capacitor V_c will be positive. Likewise, at the end of a negative cycle, V_c will have a negative value. Therefore, the Appellant contends that the load control signals are not generated separately for the first and second loads; rather, Dalnodar generates a single control signal that is merely the varying value of V_c.

Accordingly, for the foregoing reasons, Dalnodar neither describes nor renders obvious a circuit array for controlling a switch to apply voltage to first and second loads based on whether a phase of the AC voltage is positive or negative and logical load control signals generated separately for the first and second loads. Therefore, the Appellant respectfully requests the rejection of claim 6 be withdrawn.

Claim 7

Claim 7 further limits the circuit array of claim 1 requiring: "a phase detection device to detect whether a phase of the AC voltage is positive or negative and to output a logical detection signal that corresponds to the phase" and "a logic unit to generate, based on the logical load control signals and the logical detection signal, a switch control signal to control the switch."[32]

As discussed previously with regard to claim 1, Dalnodar does not describe or suggest either a logical detection signal or a logical load control signal. Accordingly, Dalnodar cannot be said to describe or suggest a logic unit to generate a switch control signal to control the switch based on those same logical signals.

Claim 19

Claim 19 further limits the circuit array of claim 1 requiring that: "the semiconductor switch on the circuit path that includes the two loads comprises a single MOSFET device." Dalnodar neither describes nor renders obvious the features of claim 19.

In contrast, Dalnodar describes the switch on the load path as being a triac (T1 in Figure 4, below).

[32] Appellant's claim 7 (emphasis added).

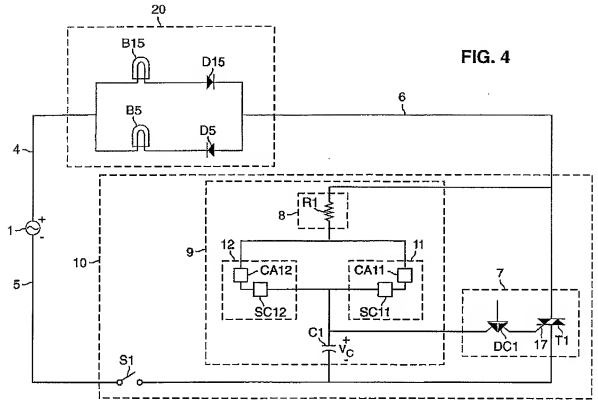


FIG. 4

In conceding that the switch T1 is not a MOSFET as required by Appellant's claim 19, the Examiner asserts that "**it would have been obvious to one skilled in the art to substitute the Dalnodar triac with a MOSFET device, since the two components are art recognized switching devices. Both the triac and MOSFET connect input and output lead lines based on a signal received at their gate.**" Appellant disagrees. A triac ("TRIode for Alternating Current") is an electronic component that is approximately equivalent to two silicon-controlled rectifiers (SCRs/thyristors) joined in inverse parallel (paralleled but with the polarity reversed) and with their gates connected together. This results in a bidirectional electronic switch which can conduct current in either direction when it is triggered and thus doesn't have any polarity. The triac can be "triggered" by either a positive or a negative voltage being applied to its gate electrode.

In contrast to the triac which conducts current in both directions depending on the gate signal, the MOSFET recited in the Appellant's claim 19 either blocks or allows current flow to the load. Because a MOSFET and a triac perform different functions, it would not have been obvious to replace the triac described in Dalnodar with the MOSFET of claim 19.

Claim 21

Claim 21 further limits the circuit array of claim 1 requiring that: "the semiconductor switch is connected between ground and the two loads." Dalnodar neither describes nor renders obvious the features of claim 21.

The Examiner contends that "**Dalnodar discloses the switch is connected between ground (5) and the two loads (20).**"[33] The Appellant disagrees. By referring to any of Figures 1, 3-4, 5b, 6a, 6b, or 7 of Dalnodar, it is clear that element 5 does not represent ground. Element 5, as expressly described by Dalnodar, is a conductor that is described as being "hot"[34] and is directly connected to a negative terminal of AC power supply 1. Since conductor 5 is a hot wire that is connected to a negative source of voltage, it cannot also be considered the grounding point of the circuit. Accordingly, Dalnodar neither describes nor renders obvious a semiconductor switch that is connected between ground and the two loads.

[33] Office Action of November 11, 2008, page 8.
[34] Dalnodar, col. 3, lines 45-50.

Claim 22

Claim 22 further limits the circuit array of claim 1 requiring that: "the logical load control signal comprises a signal selected from a group consisting of a logical 0 and a logical 1." Dalnodar neither describes nor renders obvious the features of claim 22.

In contrast to the claimed logical load control signals comprising either a logical 0 and a logical 1, Dalnodar discloses an analog signal (see discussion above in relation to claim 1). The Examiner acknowledges that the signal supplied to DC1 is an analog signal and states "**Dalnodar discloses that analog signals are passed from the phase detectors (11, 12) to the diac (DC1).**" However, in rejecting claim 22, the Examiner states "**Dalnodar discloses the diac provides a logical 0 and a logical 1 to cause the triac to switch... The diac would output a 0 and 1 regardless of where it is placed in the circuit (as the DAC connected to the output of the phase detectors or as the switch control for the triac).**"

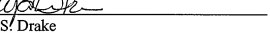
To the best of the Appellant's understanding, the Examiner appears to suggest that it would have been obvious to add two additional diacs to Dalnodar's circuit between the variable resistors VR11 and VR12 and the capacitor C1. However, as described in detail above in relation to claim 1, inserting diacs in such a location would no longer allow Dalnodar's circuit to function appropriately because the capacitor C1 would no longer be charged in the same manner. Accordingly, it would not have been obvious to place additional diacs in Dalnodar's circuit.

Conclusion

The Appellant respectfully submits that claims 1-11 and 19-22 are allowable over the art of record. Therefore, the Examiner erred in rejecting the Appellant's claims and should be reversed.

Respectfully submitted,

Date: 3/18/09



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Appendix of Claims

1. A circuit array for controlling operation of two loads that operate with a rectified AC voltage, the circuit array comprising:

a first current path that includes a first load of the two loads;

a second current path that includes a second load of the two loads;

a semiconductor switch on a circuit path that includes the two loads, the semiconductor switch being electrically connected to a common node of the first current path and the second current path; and

a control unit to generate a switch control signal that controls the semiconductor switch; wherein the control unit comprises:

a phase detection device to detect whether a phase of the AC voltage is positive or negative, and to output a logical detection signal that is based on whether the phase is positive or negative; and

a logic unit to generate the switch control signal based on one or more logical load control signals and the logical detection signal, wherein the control unit is configured to supply the first current path with a first half wave of the rectified AC voltage and to supply the second current path with a second half wave of the rectified AC voltage.

2. The circuit array of claim 1, wherein the control unit further comprises a time control circuit for generating one of the load control signals, the time control circuit generating the one of the load control signals at a predetermined time.

3. The circuit array of claim 1, wherein the control unit further comprises a sensor circuit for generating one of the load control signals, the sensor circuit generating the one of the load control signals in response to a sensed condition.

4. The circuit array of claim 1, wherein the logic unit is comprises a multiplexer that receives the load control signals and that outputs the switch control signal in response to the detection signal.

5. The circuit array of claim 1, wherein the circuit array is part of an integrated circuit.

6. An electronic device, comprising:

an input having leads to receive AC voltage;

a circuit array for controlling a switch to apply voltage to first and second loads based on whether a phase of the AC voltage is positive or negative and logical load control signals generated separately for the first and second loads; and

a rectifier that is connected to the input and that provides the voltage to the first and second loads, the voltage being generated from the AC voltage, wherein the rectifier comprises an open bridge circuit, and wherein the voltage comprises different half waves of the AC voltage wherein a first half wave of the rectified AC voltage is applied to the first load and a second half wave of the rectified AC voltage is applied to the second load.

7. The electronic device of claim 6, wherein the circuit array comprises:

a phase detection device to detect whether a phase of the AC voltage is positive or negative and to output a logical detection signal that corresponds to the phase; and

a logic unit to generate, based on the logical load control signals and the logical detection signal, a switch control signal to control the switch.

8. The electronic device of claim 6, wherein the control unit comprises a time control circuit for generating one of the load control signals, the time control circuit generating the one of the load control signals at a predetermined time.

9. The electronic device of claim 6, wherein the control unit comprises a sensor circuit for generating one of the load control signals, the sensor circuit generating the one of the load control signals in response to a sensed condition.

10. The electronic device of claim 7, wherein the logic unit comprises a multiplexer that receives the load control signals and that outputs the switch control signal in response to the detection signal.

11. The electronic device of claim 6, wherein the circuit array is part of an integrated circuit.

Claims 12-18 are withdrawn.

19. The circuit array of claim 1, wherein the semiconductor switch on the circuit path that includes the two loads comprises a single MOSFET device.

20. The circuit array of claim 1, wherein the circuit array for controlling a switch to apply voltage to the two loads is configured to:

apply a voltage to the first load of the two loads when a phase of the AC voltage is positive and

apply a voltage to the second load of the two loads when a phase of the AC voltage is negative.

21. The circuit array of claim 1, wherein the semiconductor switch is connected between ground and the two loads.

22. The circuit array of claim 1 wherein the logical load control signal comprises a signal selected from a group consisting of a logical 0 and a logical 1.

Evidence Appendix

None

Related Proceedings Appendix

None